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Design of noise tolerant circuits for modified feedthrough logic

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Abstract— **In this paper a circuit design technique to improve noise tolerant of a new CMOS domino logic family called feedthrough logic is presented. The feedthrough logic improves the performance of arithmetic circuit as compared to static CMOS and domino logic but its noise tolerant is very less. A 2-input NAND gate is designed by the proposed technique. The ANTE (average noise threshold energy) metric is used for the comparison of noise tolerance of proposed circuit with the feedthrough logic. Simulation results for a 2-input NAND gate at 0.18-µm, 1.8 V CMOS process technology show that the proposed noise tolerant circuit achieves 1.79X ANTE improvement along with the reduction leakage power.**

Keywords- Feedthrough logic (FTL); average noise threshold energy (ANTE); leakage power; sub-threshold leakage current; noise immunity curves; noise tolerant circuits.

I. INTRODUCTION

Noise immunity in digital dynamic circuits is becoming a major issue with the progress of advanced VLSI technology. Deep submicron noise is a major issue in integrated circuit design due to scaling of devices [1]. Noise is used to designate any phenomenon that causes voltage at non switching node to deviate from its nominal value [2]. The various sources of noise in deep submicron regions are crosstalk noise due to capacitive coupling between neighboring inter-connects, small variation in nominal supply voltage values, leakage current and fluctuations in device parameters due to process variation [3]. Among the various sources of noise, the sub-threshold leakage current is the most critical because it exponentially increases with continuous scaling of MOS transistor dimension [4]. Due to technology scaling the supply voltage is scaled down in each new technology; at the same time threshold voltage V_{TH} of transistor is also scaled down to achieve high performance that leads to continuous increase in sub-threshold leakage current [4]. The leakage current is also increased due to continuous reduction in gate oxide thickness. Therefore, the design of efficient noise tolerant circuit is an important issue in present day VLSI design.

Dynamic type domino logic circuits are widely used in high performance integrated circuits and they are more compact with respect to static CMOS logic [5,6] particularly when they have wide fan-in. Wide fan-in dynamic logic circuits are employed in the critical paths of high performance chips. The major limitation of domino gates is that they are having less noise tolerance as compared to static CMOS. In static CMOS the switching threshold is equal to $V_{DD}/2$ but in dynamic logic the switching threshold is equal to the threshold voltages of the pull down NMOS transistors.

The feedthrough logic (FTL) proposed in [7] is also a type of dynamic logic with certain added features that facilitates better performance compared to domino counterpart. The various limitations of domino logic like charge sharing, charge leakage etc. are also eliminated by FTL. However, FTL is also less noise tolerant. The noise tolerant property of FTL can be improved mainly by increasing the V_{TH} of NMOS transistors while they operate in evaluation phase. This is achieved by raising the source voltage of transistors to prevent the input gate from noise injection.

The rest of the sections are organized as follows, section II presents the operating principle of FTL in and modified LP-FTL [8], in section III various circuit techniques to improve noise tolerance of LP-FTL structure is described, section IV presents the noise tolerance analysis of an inverter and a 2-input NAND gate, finally conclusions are presented in section V.

II. CONVENTIONAL FTL PRINCIPLE OF OPERATION

The basic structure of FTL is shown in Fig. 1(a). It consists of a NMOS transistor (T_R), a pull up PMOS load transistor (T_{P1}) and a NMOS block. T_{P1} and T_R controlled by the clock signal (Φ). The basic operating principle of FTL presented in [7] is briefed here for continuity purpose only.

When Φ goes HIGH, (reset phase) T_R turns on and the output node (OUT) is pulled to ground through T_R. During evaluation phase i.e. when Φ goes LOW, T_R is turned off,

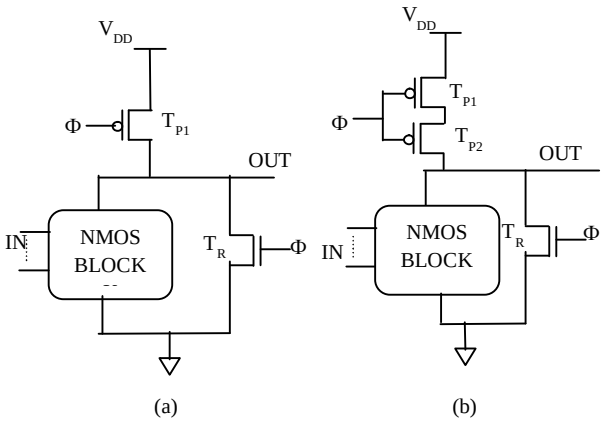

Fig. 1. Basic structure of (a) FTL [7]. (b) LP-FTL [8]

and the voltage at node OUT rises initially; then it becomes logic HIGH (i.e. $V_{OH} = V_{DD}$) or LOW (V_{OL}) depending upon input (IN) to the NMOS block. If the NMOS block evaluates to HIGH then node OUT is pulled up towards V_{DD} otherwise it would pull down to V_{OL}. So when Φ goes from HIGH to LOW, node OUT makes partial transition from V_{TH} to either V_{OH} or V_{OL} depending upon IN value.

Despite of its improvement in speed, the FTL structure suffers from non-zero nominal low output voltage i.e. $V_{OL} \neq 0$ due to contention between PMOS and NMOS during the evaluation period. This non-zero V_{OL} increases dynamic power consumption of the circuit. The V_{OL} is reduced further by using LP-FTL in [8].

The LP-FTL [8] circuit is shown in Fig. 1(b). It comprises one additional PMOS transistor T_{P2} in series with T_{P1}. The insertion of additional PMOS reduces the source voltage of T_{P2} below V_{DD}. Since T_{P1} and T_{P2} are in series the voltage at the source of T_{P2} is less than $V_{DD.}$ It is a case of ratio logic; the output node is pulled to logic low voltage i.e. V_{OL} which is less than the V_{OL} of existing FTL structure in [7]. This reduction in V_{OL} facilitates significant reduction in dynamic power consumption.

The LP-FTL in [8] is less noise tolerant because of less switching threshold which is only depends upon transistors in the NMOS block. The noise tolerant of LP-FTL is improved by increasing the switching threshold value NMOS transistors in the evaluation phase.

III. Proposed Improved Noise Tolerant Techniques

The noise tolerance of LP-FTL in [8] is improved by increasing the threshold voltage of transistor in NMOS block during evaluation phase. Fig. 2(a) shows the inverter circuit designed by LP-FTL structure. During evaluation phase, when the noise pulse at the gate of T_N has an amplitude $V_N \geq V_{TH}$, it will cause malfunction in the circuit. This can be avoided by raising the threshold voltage of $T_{N.}$ The increase in threshold voltage of NMOS transistors leads to reduction in sub-threshold leakage current [4]; as a result leakage power dissipation also decreases.

The sub-threshold leakage current is given by [4]

$$I_{subth} = A\ e^{\frac{1}{m v_T}\left((V_{GS} - V_{th0} - \gamma' V_S + \eta V_{DS})\right)}\left(1 - e^{-\frac{V_{DS}}{v_T}}\right)$$

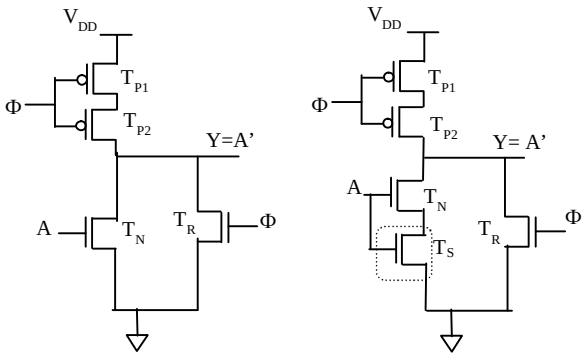

Fig. 2. LP-FTL structure (a) inverter. (b) Stacked Transistor inverter

a. Stacked Technique:

In stacked technique a single NMOS transistor is replaced by one or more series connected NMOS transistor. In Fig. 2(b) the stacked transistor T_S is used in series with T_N. Similarly for the 2-input NAND gate shown in Fig. 3(b) the two NMOS transistor T_{N1} and T_{N2} are replaced by stacked transistor T_{S1} and T_{S2} in series with T_{N1} and T_{N2} respectively as shown in Fig. 3(b). The stacked transistor reduces the sub-threshold leakage current as follows,

(i) It increases the source potential (V_S) of $T_{N,}$ as a result its gate to source voltage (V_{GS}) reduces that leads to reduction in sub-threshold leakage current (I_{subth}).

(ii) An increase in V_S causes V_{TH} of T_N to increase as a result sub-threshold leakage current also reduces.

b. Stacked transistor with pull-up PMOS transistor (Triple Transistor Technique)

A 2-input NAND gate designed by this technique is shown in Fig. 3(c) In this technique one additional PMOS transistor is used along with stacked transistor. The PMOS transistors (T_{P3}) further increases the source voltage of T_{N1} along with the stacked transistor (T_{S1}). Similarly the threshold voltage of T_{N2} is increased by T_{P4} and T_{S2} In this technique the reduction in sub-threshold leakage current is more as compared to stacked transistor technique; as a result this circuit is more noise tolerant as compared to stacked technique.

IV. Simulation Results

The noise robustness of various noise tolerant techniques is analyzed by using ANTE (average noise threshold energy) metric in [9]. ANTE is defined as the average input noise energy that the circuit can tolerate. The pulse energy is defined as energy dissipated in a 1Ω

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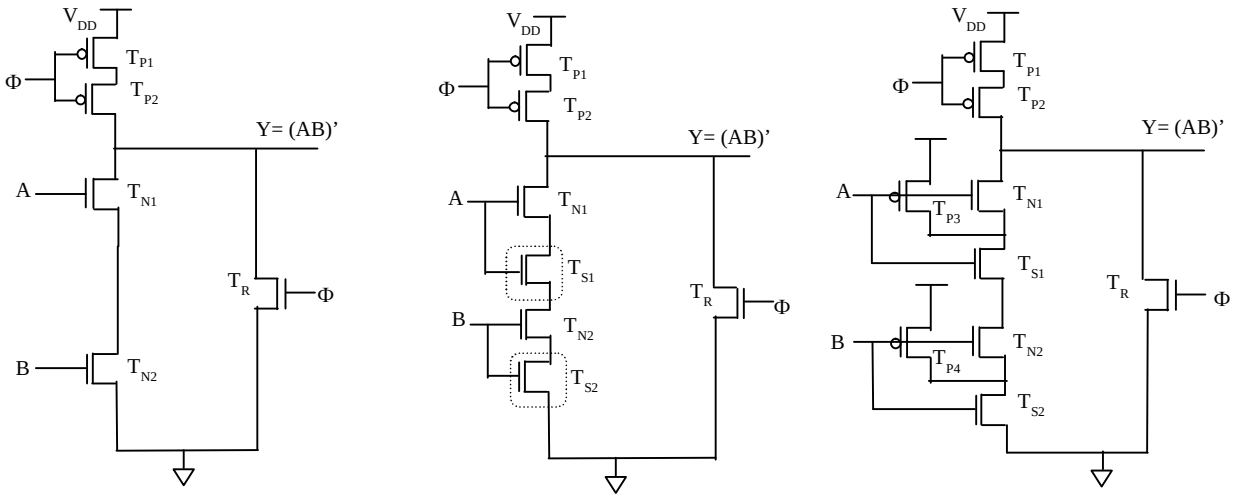
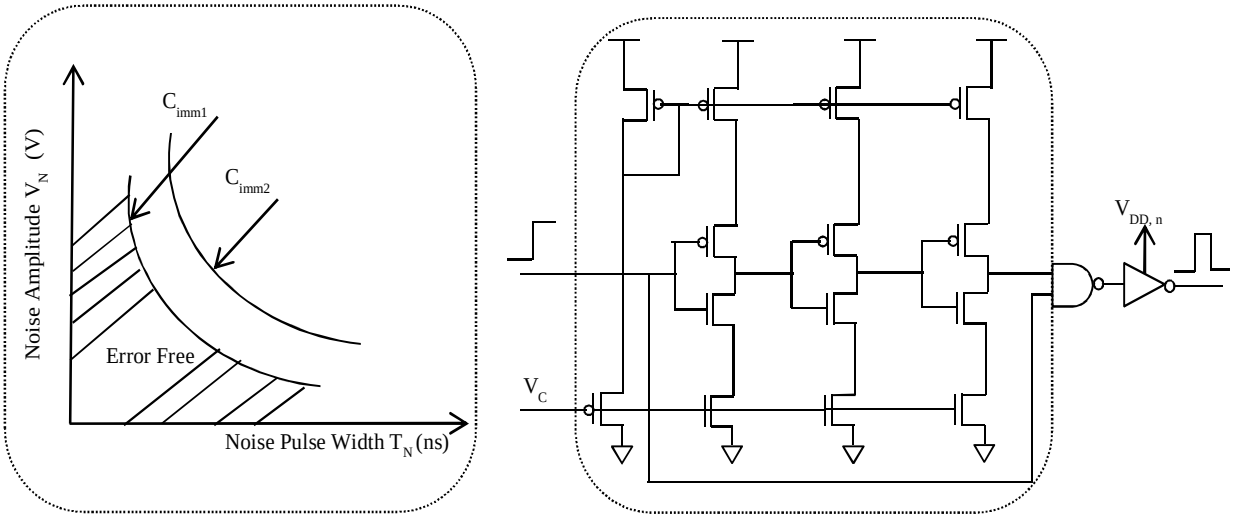


(a) (b) (c)

Fig. 3. LP-FTL structure (a) 2-input NAND. (b) Stacked Transistor NAND (c) Triple transistor NAND



(a) (b)

Fig. 4. (a) Noise immunity curve [9]. (b) NIC [10].

resistor subject to a voltage wave form of amplitude V_N and width T_N.

$$ANTE = E(V_N^2 T_N)$$

Where E ( ) denotes the average value.

The performance of various noise tolerant circuits is compared by using noise immunity curves shown in Fig.4 (a). This noise immunity curve [9] is the locus of noise amplitude (V_N) and width (T_N) combinations that cause the output of a logic gates switch. All the points on and above the curve represents the noise pulses that will change the output of logic gate from its desired value. The circuit with noise immunity curve given by C_{imm2} is more robust than one with C_{imm1}.

For measuring the noise immunity of various noise tolerant circuits noise pulses are injected to the input logic gates. The NIC circuit [10] is used to inject noise pules of desired amplitude (V_N) and width (T_N) at the input of various logic gates. The NIC circuit is shown in Fig.4 (b) is used to produce a glitch at the output of a gate by staggering its inputs in time. The noise-pulse width (T_N) produced by NIC is controlled by V_C and the amplitude of noise pulse (V_N) is controlled by the supply voltage of final inverter $V_{DD, n}$. so by varying V_C and $V_{DD, n}$ various amount of noise can be injected at the input of logic gates.

a. inverter

Fig.5. Shows the noise immunity curves for inverter designed by LP-FTL and stacked transistor technique for various V_N and T_N using 0.18µm CMOS process technology model library from UMC, using the parameter for typical process corner at 25^0 C. Since the stacked transistor reduces the sub-threshold leakage current, the inverter designed by stacked transistor technique is more robust than LP-FTL [8]. Table I shows the leakage power and ANTE comparison for the inverter. The stacked transistor technique improves the ANTE by 1.54X.

TABLE I. PERFORMANCE COMPARISON FOR INVERTER AT 180 NM TECHNOLOGY

Techniques	$P_{leakage}$ (pW)	t_p (ps)	ANTE (v^2*ns)
LP-FTL [8]	261	80	0.298
Stacked Transistor	147	83	0.460

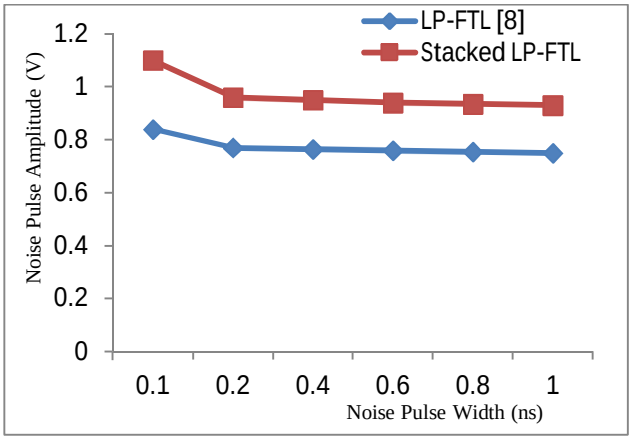


Fig.5. Noise immunity curves for inverter

b. 2-input NAND gate

The noise immunity curves for a 2-input NAND gate designed by LP-FTL structure [8], stacked transistor and triple transistor technique is shown in Fig.6 for V_{DD}=1.8V and in Fig.7 for V_{DD} =3.3V. These curves are obtained by applying the noise pulses to the input of NAND gate generated from NIC. The noise pulse width (T_N) is kept fixed while the noise amplitude is increased until the output node of NAND gate changes its logic state. This process is repeated for various T_N values. From Fig.6, we observe that the NAND gate designed by triple Transistor technique is more robust compared to the original LP-FTL structure. Table II shows the performance comparison for a 2-input NAND gate in 0.18µm CMOS process technology model library from UMC, using the parameter for typical process corner at 25^0 C. Power supply V_{DD} is constant and is equal to 1.8V. From the table, it is observed that the ANTE for triple transistor technique is improved by 1.79X over LP-FTL structure. The triple transistor technique reduces the leakage power 14% as compared to the LP-FTL structure.

Table III shows the performance comparison for a 2-input NAND gate using 0.18µm technology for a V_{DD}= 3.3 V. The ANTE for triple transistor technique is improved by 1.72X over LP-FTL structure and 1.49X over stacked technique. The noise immunity over delay for the triple transistor technique is improved by 1.9X with respect to LP-FTL.

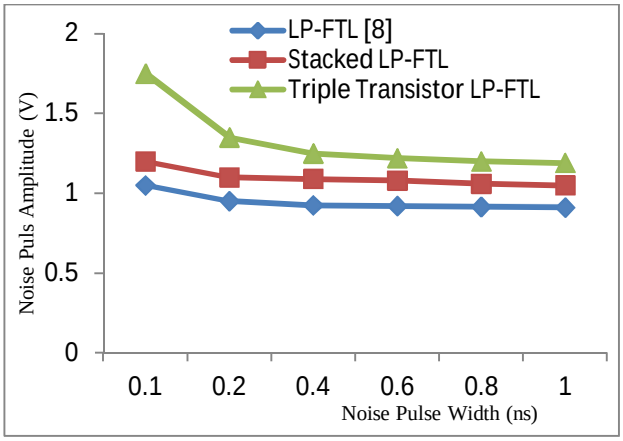


Fig. 6. Noise immunity curves for 2-input NAND (at V_{DD}=1.8V)

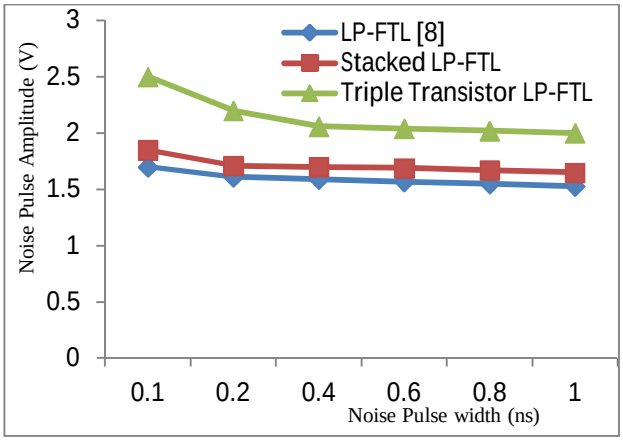


Fig. 7. Noise immunity curves for 2-input NAND (at V_{DD}=3.3V)

TABLE II. PERFORMANCE COMPARISON FOR 2-INPUT NAND AT 180 NM TECHNOLOGY (V_{DD}=1.8 V)

Techniques	ANTE (v^2*ns)	$P_{leakage}$ (pW)	Delay t_p (ns)	ANTE/Delay
LP-FTL [8]	0.439	147	0.083	5.289
Stacked Transistor	0.593	136	0.085	6.976
Triple Transistor	0.787	126	0.078	10.089

TABLE II. PERFORMANCE COMPARISON FOR 2-INPUT NAND AT 180 NM TECHNOLOGY (V_{DD}=3.3 V)

Techniques	ANTE (v^2*ns)	Delay t_p (ns)	ANTE/Delay
LP-FTL [8]	1.26	0.043	29.302
Stacked Transistor	1.460	0.044	33.185
Triple Transistor	2.175	0.039	55.782

IV. CONCLUSIONS

In this paper various noise tolerant circuit techniques are proposed to improve noise immunity of LP-FTL structure. The triple transistor techniques improves the noise tolerance of 2-input NAND gate by 1.79X and 1.35X over LP-FTL and stacked transistor techniques. With the reduction in supply voltage the noise immunity of various noise tolerant circuits reduces. The various noise tolerant circuits cause significant reduction in leakage power. The triple transistor technique reduces leakage power by 14 % with respect to LP-FTL structure along with the improvement in propagation delay.

REFERENCES

[1] K. L. shepard and V. Narayanan, "Noise in deep submicron digital design," *in Proc. ICCAD*, pp. 524-531,1996.

[2] K. L. shepard, "Design methodologies for noise in digital integrated circuits," *in Proc. DAC'*, pp. 94-99,1998.

[3] C. Murthy, "Process variation effects on circuitperformance: TCAD simulation of 256-Mbit technology," *IEEE Trans, Computer-Aided Designof integrated Circuits*, vol. 16, pp. 1383-1389, Nov.1997.

[4] K.S. Yeo, K. Roy, 'Low- Voltage, Low-Power VLSI Subsystems'.

[5] J.M. Rabaey, A. Chandrakasan, B. Nikolic, 'Digital Integrated Circuits: A Design perspective' 2e Prentice-Hall, Upper saddle River, NJ, 2002.

[6] S. M. Kang, Y. Leblebici, 'CMOS Digital Integrated Circuits: Analysis & Design', TATA McGraw- Hill Publication, 3e, 2003.

[7] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, " Analysis of high performance fast feedthrough logic families in CMOS," *IEEE Trans. Cir. & syst. II*, vol. 54, no. 6, pp. 489-493, Jun. 2007.

[8] S. Sahoo, K. Mahapatra, "Performance Analysis of Modified Feedthrough Logic for Low Power and High Speed," *in proc. IEEE-ICAESM*, pp.352-356, Mar. 2012.

[9] L. Wang and N. Shanbhag, "An energy-efficient noise-tolerant dynamic circuit design," *IEEE Trans. Cir. & syst. II*, vol. 47, pp. 1300-1306, Nov. 2000.

[10] G. Balamurugan and N. R. shanbhag, "The twin-transistor noise tolerant dynamic circuit technique," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 273-280, Feb. 2001.