International Journal of Conceptions on Electronics and Communication Engineering
Vol. 5, Issue. 1, May' 2022; ISSN: 2357 - 2809

Low Power Design of 4-bit Simultaneous Counter Employing Digital Switching Circuits for Low Range Counting Application

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Abstract— **To reduce power usage, increase battery life, and improve system performance, a low-power VLSI circuit is produced as a result.**

One of the most important factors in scaling up or scaling down any system is the counter's capacity to keep track of changes in an operator's values over time. During the counting process, the frequency and time may be changed. The power supply is the most significant challenge in scaling circuits. Consumption as a result of the clock's power dissipation mode of inactivity.The use of electricity accounts for one-third of total energy usage in a counter of the clock signal.The word "power" is used a lot in this work. By reducing the number of people in a room, consumption is minimised. Changing tasks The counter's energy usage The power consumption of flipflops can be lowered even more. This might be possible.

Keywords-low poser design; 4 bit simultaneous counter; digital switching circuits; low range counting application;

I. INTRODUCTION

The stable state of a Flip-Flop is either zero or one. It's a popular way to save the data. Flip-Flop is a fundamental construct in sequential logic.element for storing. A scaling circuit is a piece of electronic equipment that allows you to scale up or down the size of yourkeeps track of how many times a process or event has occurred.happened as a result of the clocksignal. It's put to good use.in a certain span of time the design that uses the least amount of resources.It's almost essential to have maximum power and reliability.Especially when a clock is used. Consequently, power dissipation in the circuit is kept to a minimal by using the basics of complementary metal-oxide semiconductor VLSI architecture in the clock.

II. PRESENT SYSTEM OF FLIP-FLOP AND COUNTER

A. Flip-Flop

The Flip-Flop was created using the True Single Phase Clock approach. TSPCL's primary goal is to complete the required Flip-Flop operation uses the least amount of energy and runs on The D Flip-Flop design with TSPCL delivers the maximum speed. When D is zero and CLK is at a low level, consider transistors P1 and P2. P2 is turned on, which turns on the N2 transistor in the circuit. The following phase the stage's P3 is active here, and it returns 1 as a result. Inverts to 0 D's input is similarly transformed. Every stage is inverted, and the output is identical to that of the original input.

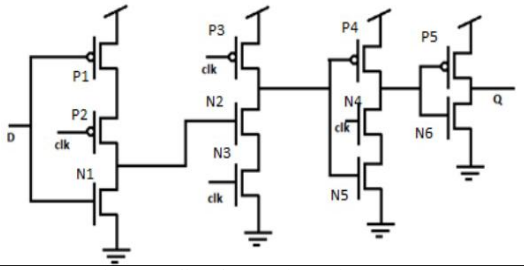

Fig 1. D Flip-Flop Design using TSPCL.

The top SVL is composed of two NMOS in series with a parallel PMOS. Two NMOS connected to the supply provide the gate to PMOS, which in turn gets the clock from the input clock bar. It is possible to activate PMOS by setting the clk to 1, which in turn turns on clkb to 0. As a result, the PMOS begins to conduct and can cross the supply voltage 1. When clk is zero and clkb is one, the two NMOS begin to conduct and are connected to the ground. The leakage power of the circuit can be minimised by connecting the NMOS in series when it is turned off. Upper SVL is shown in below Figure 2.

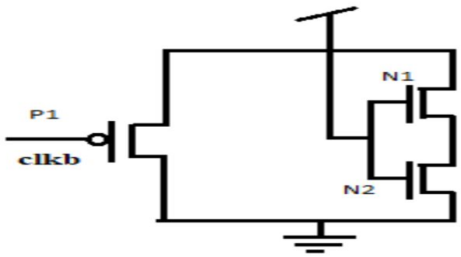

Fig 2. Upper SVL Design.

There are two PMOS in the bottom SVL, followed by an NMOS in series. The input clock is linked to the gates of the two PMOS, while the NMOS gate is grounded. When the clk value is 1, NMOS is disabled. Consequently, the PMOS begin to conduct and connect to the planet. When the clock is stopped at zero, the two NMOS start conducting, which allows supply voltage 1 to flow through the circuit. The bias of the circuit is reversed when PMOS are coupled in series, which results in lower leakage current while the device is in standby mode. A commonly used CMOS D Flip-Flop circuit in both analogue and digital systems. CMOS is an integrated circuit type. Lower SVL is seen in Figure 3 below.

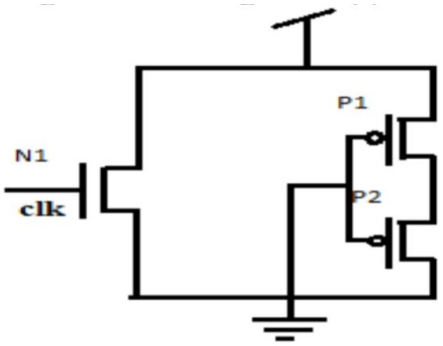

Fig. 3.Lower SVL Design.

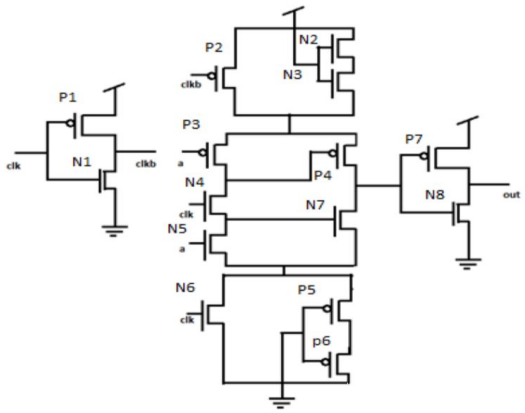

Fig. 4.Design of D Flip-Flop with Modified SVL.

There is activation of P1 and activation of N2 and deactivation of P2, P3 as well as deactivation of N1 and N2. D Flip-Flop must be used for this. Both the ground and the power supply are present. If P1, N1, N3, and P2, N2 are all passive, then nothing will happen. No longer an issue. P1 is formed when an equals 1. While activating N1, N2, and P2, N3 is rendered inactive. From this condition, one arises. P1 and N3 are disabled. Open N1 and N2 circuits are both active, but when the supply voltage increases, so does the supply voltage. Because it functions as a pull-up network, it generates Vdd-Vth. When you connect the NMOS transistors in series, you get Static power is reduced. P2, P3, and P4 are active, but they do not provide any information. positive voltage of a finite amount. Fig.4 shows the D Flip-Flop with SVL Modifications in action.

B. Counter Design

Due to clock gating, a power-saving simultaneous counter is created. Because of this logic, When the Flip-Flops are activated, the clock just switches state. The issue of the circuit's complexity. A power-efficient simultaneous counter is created. Due to clock gating the system is more efficient. Because of this logic when the Flip-Flops are activated, the clock just switches state. The issue of The circuit's complexity.

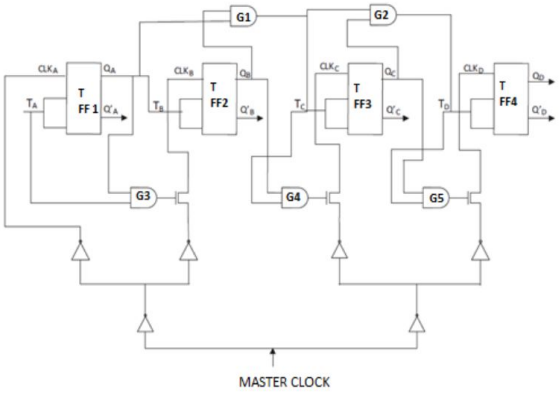

Fig. 5.Block Diagram of 4-Bit Existing Binary Up Counter

This design may be used with a wide range of components. In response to the clock network, the Flip Flop gets a clock signal. Serially connecting repeaters prevents clock skew in this method. The clock network of the circuit uses less energy because of a combinational logic that regulates the clock depending on Flip-Flop activity. Therefore, power may be optimised by minimising unnecessary clock activity during the idle Flip-Flop. Figure 5 depicts the architecture of a 4-Bit Existing Binary Up Counter.

III. RESEARCH METHOD OF FLIP-FLOP AND COUNTER DESIGN

The proposed T-flip-SVL flop's and SVD designs are combined here. A positive edge activates a Flip-Flop in the method described below. Less power is used by the TSPCL and SVL technologies compared to a standard Flip-Flop. There is activation of P1 and N2 as well as deactivation of P2 and P3.

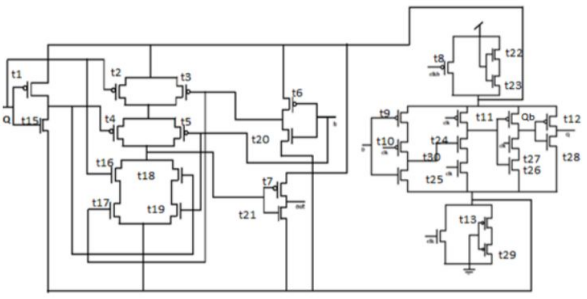

Fig. 6.Design of the Proposed T Flip-Flop with SVL.

To accomplish the task, It is coupled to power and GND for standard D Flip-Flop operation. When is inactive, P1, N1, N3, and P2, N2 take on their active roles. Out gets inactive because they are inactive. a = 1 P1, N3 become inactive, whereas N1, N2 become active. out of the P2 active state N3 and P1 are both present. open circuits in the off state Although N1 and N2 are active, Because they work as a pull-up, the supply voltage is Vdd-Vth. network.FIG. 6 depicts the design of the proposed T-Flip-Flop with coupled SVL construction.

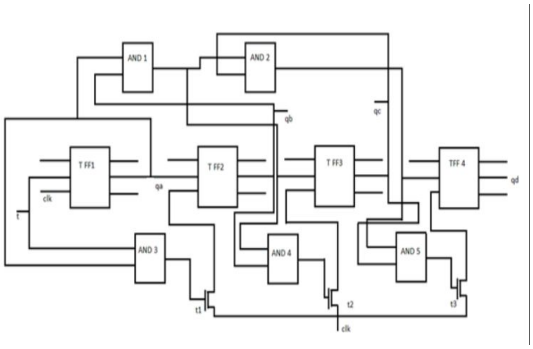

Fig. 7.Counter Design Proposed Using a Modified Flip-Flop.

This system features a T Flip-Flop cascade structure. The adoption of T Flip-Flop is inspired by environmental considerations. changing the activity of the following state It turns off the clock. When the flip-input flop's is zero, the transition happens. When the clock is zero, it has no influence on the circuit's output; hence, the output remains in its previous state. However, when the clock is set to one, the output is toggled. Consequently, it is evident that the clock controls the counter. Figure 7 is a block representation of the suggested countermeasure.

IV. Results and Discussion

Tanner EDA TOOL was used to simulate all of the designs at various supply levels utilising the 250nm CMOS technology library.

A. Simulation of Flip-Flop and Counter Results

TSPCL and SVL were used to simulate the proposed T Flip-Flop design, as illustrated in the accompanying Fig. 8.

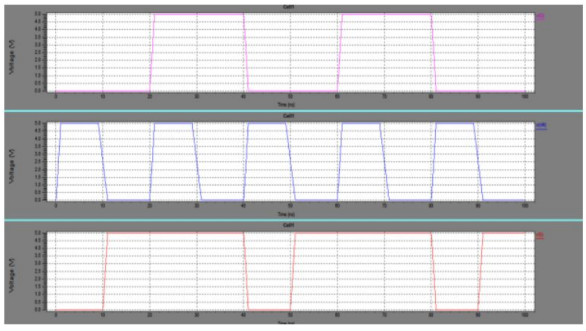

Fig. 8 T Flip-Flop Waveform with Combined SVL.

CLK is the clock input, while b is the input for it. Input is 0 and output is 0 when clock's first positive edge comes around. It was on the second rising edge that the result went from 0 to 1 while the output stayed steady. Because the input is 1 during the clock's third rising edge, the output is toggled from 1 to 0 on the clock's falling edge, and the output remains stable. edge. The output toggles from 0 to 1 on the next rising edge of the clock signal, and the output stays the same on the falling edge.

Using proposed T Flip-Flop the counter of simulation result is shown in below fig.9.

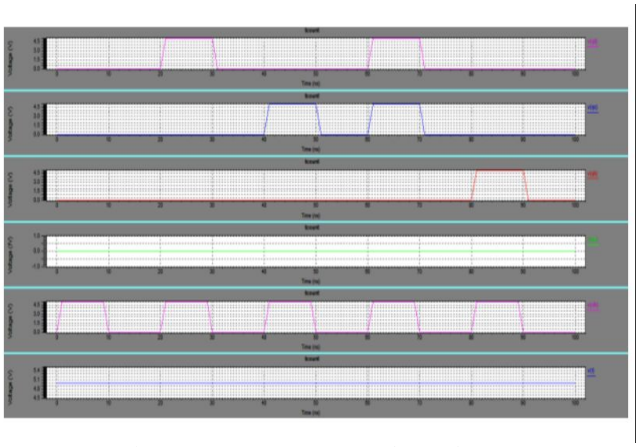

Fig.9.Countermeasure Proposed Waveform.

B. Power Comparison Results of Flip-Flop and Counter.

Table - I: Result of Flip-Flop Design Consumption at Various Supply Voltages

FLIP-FLOP DESIGN	AVERAGE POWER CONSUMPTION IN WATTS					
	2.5V	3V	3.5V	4V	4.5V	5V
T Flip-Flop with TSPCL	0.14	0.22	0.52	0.80	0.90	1.21
T Flip-Flop with SVL	0.11	0.14	0.42	0.62	0.71	0.84
T Flip-Flop with combined SVL	0.07	0.11	0.23	0.34	0.54	0.68

It is possible to compare the power dissipation of different Flip-Flop and counter architectures at various supply voltages. Using TSPCL and SVL, a Flip-Flop design is shown in Table I, with power dissipation. The power consumption of several Flip-Flop and counter architectures is compared for various supply voltages. Table I compares the current and proposed counters' power dissipation results for supply voltages between 2.5V and 5.0V.

Table – II: Four-Bit Up-Counter Power Consumption at Various Supply Voltages

COUNTER DESIGNS	AVERAGE POWER CONSUMPTION IN WATTS					
	2.5V	3V	3.5V	4V	4.5V	5V
Existing counter	3.27	3.98	4.65	5.34	6.23	6.82
Proposed counter	2.18	2.92	3.33	3.91	4.45	4.68

Table-II demonstrates that the suggested counter design reduces power dissipation by 33%.

V. CONCLUSION

Reduces counter power consumption by implementing the T Flip-Flop with Clock Gated Approach as recommended. The T Flip-Flop combines TSPCLL and SVL. Compared to the existing design, the T Flip-Flop consumes just 0.34 microwatts of energy, a decrease of 30 percent. The new counter design consumes 27 percent less energy than the existing counter design. The Tanner Tool was used to develop and simulate the T Flip-Flop and counter using CMOS 250nm technology. To increase battery life, the recommended counter minimises power consumption and chip area. Using the TSPCL, the Upper and Lower SVL, and an external power source, a Flip-Flop may be constructed.

REFERENCES

[1] C. Christakis, G. Theodoridis and A. Kakarountas, "High speed binary counter based on 1d cellular automata," 5th International conference on modern circuits and systems technologies (MOCAST), Thessaloniki, pp. 1–4, 2016.

[2] K. Gavaskar and U S. Ragupathy, "Low power self-controllable voltage level and low swing logic based 11T SRAM cell for high speed CMOS circuits," Springer, Vol. 100, No. 1, pp. 61-77, 2019.

[3] T. Doi, and V. Niranjan, "Low power and high performance ring counter using pulsed latch technique," International conference on micro-electronics and telecommunication engineering (ICMETE), Ghaziabad, pp.584–586, 2016.

[4] M. Gautam, U. Nirmal and R. Jain, "Low power sequential circuits using improved clocked adiabatic logic in 180nm CMOS processes," International conference on research advances in integrated navigation systems (RAINS), Bangalore, pp.1–4, 2016.

[5] K. Gavaskar, U S. Ragupathy and V. Malini, " Design of Novel SRAM cell using Hybrid VLSI Techniques for Low Leakage and High Speed in Embedded Memories," Springer, Vol. 108, No.4, pp.2311-2339, 2019.

[6] YT. Hwang and JF. Lin, "Low voltage and low power divide-by-2/3 counter design using pass transistor logic circuit technique," IEEE Trans Very Large Scale Integrating VLSI System , Vol. 20, No. 9, pp. 1738–1742, 2012.

[7] K. Gavaskar, U S. Ragupathy and V. Malini, "Proposed Design of 1KB Memory Array Structure for Cache Memories," Springer, pp.1- 29, ISSN : 1572-834X (online).

[8] JS. Kim, JO. Yoonand and B D. Choi, " Low-power counter for column-parallel CMOS image sensors," IEEE Asia Pacific conference on circuits and systems (APCCAS), Jeju, pp.554–556, 2016.

[9] K. Gavaskar and U S. Ragupathy, " An efficient design and analysis of low power SRAM memory cell for ULTRA applications," Asian journal of research in social sciences and humanities, Vol. 7, pp. 962- 975, 2017.

[10] Madhu Shakya and Shweta Agrawal, "Design of Low Power C-MOS D flip-flop using modified SVL technique," International Journal of Research and Analytical Reviews, Vo. 5, No. 4, pp. 2349-5138, 2018.

[11] E. Ogunt, M. Frank and S. Foo, "Design of a low power binary counter using bi-stable storage element," International conference on electronic design, Penang, pp.1–5 , 2008.

[12] K. Gavaskar and U S. Ragupathy, "An efficient design and comparative analysis of low power memory cell structures," IEEE International conference on Green Computing, Communication and Electrical Engineering (ICGCCEE'14), pp. 489-493, 2014.

[13] Priyanka Sharma and Rajesh Mehra, "True single phase clocking based flip-flop using different foundries," International Journal of Advances in Engineering and Technology, Vol. 7, No. 2, pp. 352- 358, 2014.

[14] K. Gavaskar and S. Priya, "Design of efficient low power stable 4-bit Memory cell," International journal of computer applications, Vol. 84, pp. 0975-8887, 2013.

[15] JM. Rabaey, A. Chandrakasan and B. Nikolic, "Digital integrated circuits- A design perspective," 2013.

[16] Raghava Katreepalli and Themistoklis Haniotakis, "Power efficient synchronous counter design," ELSEVIER, Vol. 75, pp. 288–300, 2019.

[17] K. Gavaskar and S. Priya, "Design of Efficient Low power 9T SRAM cell," International Journal of Engineering Research and Technology, Vol. 2, No.1, pp. 2278-0181, 2013.