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Low Power Testing Techniques for Ultra Power Based SoC System

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Abstract— **To find the proper solutions for test power reduction strategy for parallel core-based SoC, in this paper, starting from the terminology and models for power consumption during test, The efforts to reduce the power consumption during normal function mode further exaggerated the power consumption problem during test. The state of the art in low-power testing is presented, various power reduction techniques proposed for all aspects of testing like external testing, Built-In Self-Test techniques, and the advances in LFSR techniques emphasizing low power. Further, all the available low-power testing techniques are strongly analyzed. To reduce the cost and time to market, the modular design approach is largely adopted for system-on-chip.**

Keywords-SoC System, low power, ultra power

I. INTRODUCTION

In general, power reduction can be implemented at different levels of design abstraction: system, architectural, gate, circuit and the technology level. At the system level, inactive modules may be turned off to save power. At the architectural level, parallel hardware may be used to reduce global interconnect and allow a reduction in supply voltage without degrading system throughput. Clock gating is commonly used at the gate level. A variety of design techniques can be used at the circuit level to reduce both dynamic and static power. The power consumption has been a major challenge to both design and test engineers.[2] The efforts to reduce the power consumption during normal function mode further exaggerated the power consumption problem during test. Generally, a circuit may consume 3–8 times power in the test mode than in the normal mode. With ever increasing System-on-Chip (SoC) complexity, energy consumption has become the most critical constraint for today's integrated circuit (IC) design. Consequently, a lot of effort is spent in designing for low-power dissipation. Power consumption has become a primary constraint in design, along with performance, clock frequency and die size. Lower power can be achieved only by designing at all levels of abstraction: from architectural design to intellectual property (IP) component selection and physical implementation. Energy reduction techniques can also be applied at all levels of the system.

II. POWER MINIMIZATION TESTING METHODS

1.1 A high density system like ASIC or SoC always demands the nondestructive test which satisfies all the power constraints defined during design phase.[1]

1.2 An their way, the current testing philosophy demands much more power consumption during test compared to power consumption during functional mode. This section describes the reasons and effects of such high-power consumption.

1.3. Reasons of High-Power Consumption during Test. There are several reasons for this increased test power. Out of them, the main reasons are as follows.

1.4. The test efficiency has been shown to have a high correlation with the toggle rate; hence, in the test mode, the switching activity of all nodes is often several times higher than the activity during normal operations. One of the most effective ways of reducing power at the technological level is to reduce the supply voltage, because the power consumption drops quadratically with the supply voltage. However, lowering supply voltage results in reduction of performance; therefore, any such voltage reduction must be balanced against any performance drop. To compensate and maintain the same throughput, extra hardware can be added.This can only be successful to the point where the additional circuitry does not diminish the savings.

III. LOW-POWER TEST

A high density system like ASIC or SoC always demands the nondestructive test which satisfies all the power constraints defined during design phase. On the other way, the current testing philosophy demandsmuch more power consumption during test compared to power consumption during functional mode. This section describes the reasons and effects of such high-power consumption.

2.1. Reasons of High-Power Consumption during Test. There are several reasons for this increased test power. Out of them, the main reasons are as follows.

(i) The test efficiency has been shown to have a high correlation with the toggle rate; hence, in the test mode, the switching activity of all nodes is often several times higher than the activity during normal operations.

(ii) In an SoC, parallel testing is frequently employed to reduce the test application time, which may result in excessive energy and power dissipation.

2.2. Effects of High-Power Dissipations. The most adverse effect of very high-power dissipation during test is the destruction of IC itself. In addition, to prevent the IC from destruction, the power dissipation during test can affect the cost, reliability, autonomy, performance-verification, and yield-related issues [4]. Some of the effects are as follows.

(i) The growing need of at-speed testing can be constrained because of the high-power dissipation. So stuck at faults can be tested without any effect, but the testing of the delay fault will become difficult.

(ii) During functional testing of the die just after wafer etching, the unpackaged bare die has very little provision for power or heat dissipation. This might be a problem for applications based on multichip module technology, for example, in which designers cannot realize the potential advantages in circuit density and performance without access to fully tested bare dies [5].

2.3. Definitions and Models of Energy and Power. Power consumption in CMOS circuits can be classified into static and dynamic. Static power dissipation is due to leakage current or other current drawn continuously from the power supply. A good approximation of the energy consumed during one clock period is

$$E_i = \square S_i \square F_i \square C_o \square V^2 V_{DD} \ldots\ldots\ldots\ldots\ldots(1)$$

where S_i is the number of switching during the period, F_i is the fan out of the node, and Co is the minimum size parasitic capacitance of the circuit. The fan out of the nodes is defined by circuit topology, and the switching can be estimated by a logic simulator.The product S_iF_i is named Weighted Switching Activity (WSA) of node I and represents the only variable part in the energy consumed at node i during test application. So the energy consumed in the circuit after application of a pair of successive input vectors $(Vk-1, Vk)$ can be expressed by

$$E_{VK} = \square F_i \square C_o \square V^2_{DD} \square \Sigma_I S(i, k) \ldots\ldots\ldots\ldots(2)$$

where i ranges all the nodes of the circuits and $S(i, k)$ number of switching provoked, by Vk at node i. Consider now a pseudorandom test sequence of L vectors which is the test length. The total energy consumed in the circuit is

$$E_{total} = * Fi * C_o * V^2_{DD} * \Sigma_L \Sigma_I S(i, k), \ldots\ldots\ldots(3)$$

It should be noted that energy is the total switching activity generated during test application and has impact on the battery lifetime during power up or periodic self test of battery-operated devices. Therefore, we can express the instantaneous power consumed in the circuit after application of vectors (V_k-1, V_k) as

$$P_{inst}(Vk) = E_{Vk}/T. \ldots\ldots\ldots\ldots\ldots\ldots(4)$$

The peak power consumption corresponds to the maximum of the instantaneous power consumed during the test session. It therefore corresponds to the highest energy consumed during one clock period, divided by T. More formally, it can be expressed by

$$P_{peak} = \max_k [P_{inst}(V_k)] = \max_k (E_{Vk})/T \ldots\ldots (5)$$

Finally, the average power consumed during the test session is the total energy divided by the test time and is given as follows:

$$Pavg = E_{total}/L \cdot T. \ldots\ldots\ldots\ldots\ldots\ldots (6)$$

Elevated average power adds to the thermal load that must be vented away from the device under test. It may cause structural damage to the silicon (hot spots), to bonding wires, or to the package.

According to the above expressions of the power and

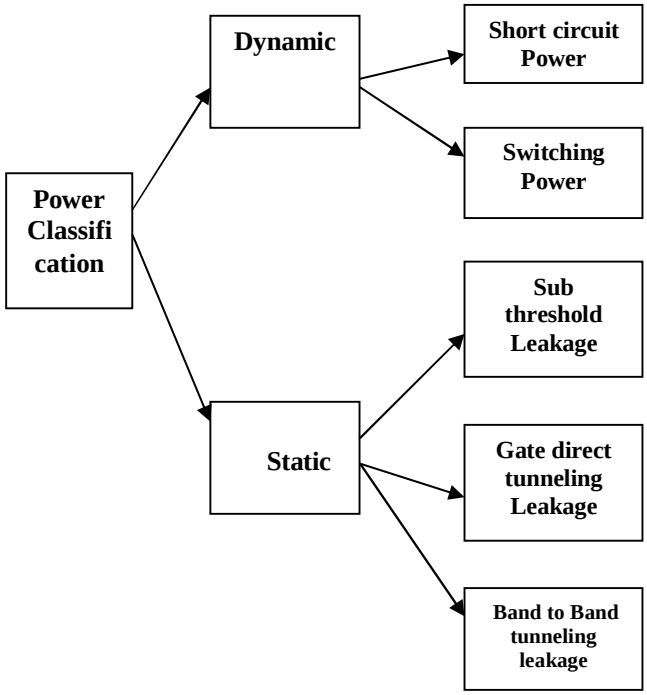

Figure 1 Sources of power consumption

IV. Low Power Reduction Schemes

During the last two decades, the number of power reduction techniques for testing has evolved. These techniques either explore the ATPG or deal with the test vectors to be used with external testing or explore the internal structure of design using BIST or DFT. So existing low-power testing scheme is divided into the following two categories.

(1) Low-Power Testing Techniques for External Testing using ATE, ATPG, and so forth.

(2) Low-Power Testing Techniques for Internal Testing using BIST, DFT, and so forth.

3.1. Low-Power Testing Techniques for External Testing.

The following are the classifications of low-power techniques for external testing.

3.1.1. Low-Power ATPG Algorithms. This power

Category contains various techniques adopted to reduce the power consumption during external testing by ATE. These methods depend on the number of transitions in test data set. The current research in this field focuses on ATPG algorithm which not only gives maximum fault coverage but also ensures the maximum fault coverage at lowest possible power dissipation. Reference [6] proposed a heuristic method to generate test sequences which create worst-case power droop by accumulating.

3.1.2. Input Control. Here the idea is to identify an input control pattern such that, by applying that pattern to the primary inputs of the circuit during the scan operation, the switching activity in the combinational part can be minimized or even eliminated. The basic idea of input control technique with existing vector- or latch-ordering techniques that reduces the power consumption has been covered in [9].

3.1.3. Ordering Techniques. The researches have widely explored the test vector reordering techniques to reduce the switching power. Hamming distance based reordering is described in survey paper [6]. Girard's approach of vector ordering is enhanced in, another method based on artificial intelligence is proposed to order the test vectors in an optimal manner to minimize switching activity during testing.

3.1.4. Exploring the Do Not Care Bit. ATPG-generated un-compacted test data contains a large number of do not care bits. [14] Proposed an automatic test pattern generation

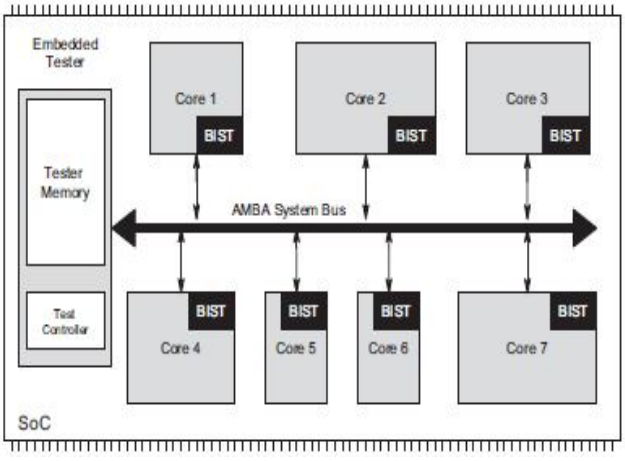

Fig. 1 AMBA bus-based hybrid BIST architecture

(ATPG) scheme for low-power launch-off-capture (LOC) transition test. The authors in [5] have used a Genetic algorithm-based heuristic to fill the do not cares. This approach produces an average percentage improvement in dynamic power and leakage power over 0-fill, 1-fill, and Minimum transition fill (MT-fill) algorithms for do not care filling. Based on the operation of a state machine, [7] elucidates a comprehensive frame for probability-based primary-input dominated X-filling methods to minimize the total weighted switching activity (WSA) during the scan capture operation. The authors in [8] describe the effect of do not care filling of the patterns generated via automated test pattern generators, to make the patterns consume lesser power. It presents a tradeoff in the dynamic and static power consumption.

3.2. Low-Power Testing Techniques for Internal Testing. The following are the classifications of low-power techniques for internal testing.

3.2.1. By LFSR Architecture. The Built-In Self-Test (BIST) architecture contains two major components: test pattern generator and response checker [9]. Both of these components use Linear Feedback Shift Register (LFSR). The LFSR can be designed to reduce the power consumption during test in the following ways.

3.2.2. By Reducing the Transitions. These methods reduce the transitions between successive patterns generated by LFSR as well as between the successive bits in a given pattern. A dual-speed LFSR scheme [2] is based on two different speed LFSRs to decrease the circuit's overall internal activity. Its objective is to decrease the circuit's overall internal activity by connecting inputs that have elevated transition densities to the slow-speed LFSR. This strategy significantly reduces average power and energy consumption without decreasing fault coverage.

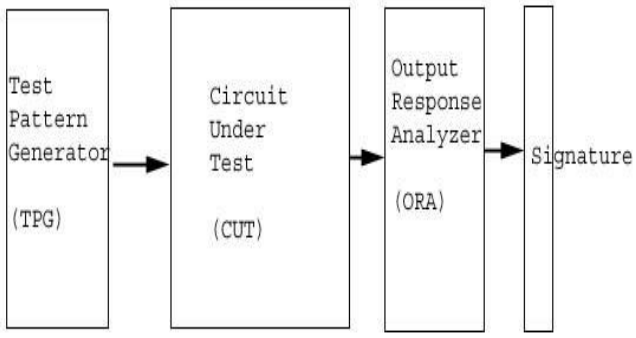

Figure 2.Basic BIST Architecture Block Diagram

The proposed BIST TPG decreases transitions that occur at scan inputs during scan shift operations and hence reduces switching activity in the CUT. In LT-LFSR [9], transitions in LFSR are reduced in two dimensions: (1) between consecutive patterns and (2) between consecutive bits. The proposed architecture increases the correlation among the patterns generated by LT-LFSR with negligible impact on test length.

An efficient algorithm to synthesize built-in TPG from low-power deterministic test patterns without inserting any redundancy test vectors is present edit [3]. The structure of TPG is based on the nonunion form cellular automata (CA). And the algorithm is based on the nearest neighborhood model, which can find an optimal non uniform CA topology to generate given low-power test patterns. A low-power dynamic LFSR (LDLFSR) circuit [11] achieves comparable performance with less power consumption. Typical LFSR, a DFLSR[I], and a LDL FSR are compared on randomness property and inviolability property. Multilayer perception neural networks are used to test this LFSRs' inviolability property.

3.2.3. By Generating the Useful Vectors Only. A significant amount of energy is wasted in the LFSR and in the CUT by useless patterns that do not contribute to fault dropping. LFSR tuning modifies the state transitions of the LFSR such that only the useful vectors are generated according to a desired sequence [2]. To reduce such energy consumption on, a mapping logic is designed in [9] which modifies the state transitions of the LFSR such that only the useful vectors are generated according to a desired sequence.

3.2.4. By Filtering Unnecessary Vectors. There are some non detecting sequences generated by LFSR. By inhibiting such vectors during testing, over all switching can be reduced. A test-vector-inhibiting technique to filter out some non detecting subsequences of a pseudorandom test set generated by an LFSR is proposed in [9].

The repeated part, which is common among some of the vectors, is not changed during the new scan path, where new test vector will be filled. As a result, the test vector is applied to the circuit under test in a fewer number of clock cycles, leading to a lower switching activity in the scan path during test mode.

V. CHARACTERISTICS OF POWER REDUCTION SCHEME SUITABLE TO UITRA POWER -BASED SOC.

(i) It should not demand the knowledge of internal structure of design.(ii) It should not make any modification in internal design.(iii) But it can add the hardware as per requirement without modifying the available I/O pin configuration.

(iv) It should deal with readymade test sequence rather than test architecture.(v) It should not be dependant on testing tools like ATPG or fault simulation which deals with the net list of design. Now comparing the available techniques with above characteristics.

4.2. Modification in LFSR. The implementation of this method

(i) deals with test sequence rather than test architecture, (ii) requires the knowledge of internal details of design, (iii) requires the additional hardware to modify test pattern sequence, and (iv) Requires modification in internal structure.

4.3. Partitioning the Circuit. The implementation of this method

(i) deals with test architecture rather than test sequence, (ii) requires the well-defined internal hierarchical structure of design, (iii) requires the knowledge of internal details of design, (iv) requires the additional hardware to modify test pattern sequence, and (v) requires modification in internal structure.

4.4. Separate Testing Strategy for Memory. The implementation of this method

(i) can be applied for memory when and where it is required, and

(ii) is not applicable to functional blocks.

4.5. Improved ATPG Algorithms. The implementation of this method

(i) deals with generation of new test set rather than available test sequence or test architecture,

(ii) requires the netlist of the design. It cannot be directly applicable to hard core, and

(iii) requires the knowledge of internal details of design.

4.6. Input Control. The implementation of this method

(i) deals with test architecture rather than test sequence,(ii) requires the knowledge of internal details of design,(iii) requires the additional hardware to modify test pattern sequence, and

(iv) requires modification in internal structure.

VI. CONCLUSION

Very advanced techniques available for power reduction during test are described in detail. The issues related to test power reduction in case of IP core based SoC are discussed, and characteristics of ideal scheme suitable to IP core-based SoC is defined. Based on that, each available category of power reduction is compared with this ideal model. It is concluded that "ordering techniques" and "exploring do not care bits" methods are the best suited to IP core-based SoC. The research can start with improvement in these schemes in terms of power reduction and then further optimizing them with other important test parameters like test application time, on-chip area overhead, test data compression, and so forth.

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